Amendments to the Claims:

Please use the following listing of claims to replace all prior versions, and listings, of the claims in the above-identified application.

Listing of Claims:

CLAIM 1 (original)

A method for fabricating complementary vertical bipolar junction transistors comprising the steps of:

providing a sapphire substrate;

forming a layer of silicon on said sapphire substrate;

recrystalizing said silicon layer;

forming a P+ region in said silicon layer to become a collector for a PNP transistor;

forming N+ region in said silicon layer to become a subcollector for an NPN transistor;

forming an N silicon layer over said P+ and N+ regions to become an intrinsic base region for said PNP transistor and to become a collector region for said NPN transistor;

forming islands of what is to become said PNP transistor and of what is to become said NPN transistor by removing any silicon therebetween to said sapphire substrate;

forming a P intrinsic base region in said N collector region for said NPN transistor;

forming P+ extrinsic base regions in said P intrinsic base region for said NPN transistor;

forming a P+ emitter region in said N base region for said PNP transistor;

forming an N+ emitter region on said P base region for said NPN transistor;

forming N+ extrinsic base regions in said N base region for said PNP transistor; and

forming individual conducting metal contacts with said emitters and extrinsic bases, said individual conducting metal contacts being formed between oxide regions.

CLAIM 2 (original)

The method according to claim 1 wherein said recrystalization is done by a double solid phase epitaxy technique.

CLAIM 3 (original)

The method according to claim 1 wherein said silicon layer formed on said sapphire substrate is approximately 0.3 micrometers thick.

CLAIM 4 (original)

The method according to claim I wherein said N, N+, P and P+ regions are created through ion implantation.

CLAIM 5 (original)

The method according to claim 1 wherein said –type silicon layer is approximately 2.5 micrometers thick.

CLAIM 6 (original)

The method according to claim 1 wherein arsenic ion implantation is used to produce said –type and N+-type regions.

CLAIM 7 (original)

The method according to claim 1 wherein boron ion implantation is used to produce said P-type and P+-type regions.

CLAIM 8 (previously presented)

The method of claim 1 further including the steps of:

forming a P+ collector plug region in said N base region for said PNP transistor so that said P+ collector plug region is incorporated into said P+ collector for said PNP transistor;

forming an N+ collector plug region in said P intrinsic base region for said NPN transistor so that said N+ collector plug region is incorporated into said N collector region of said N+ sub-collector region for said NPN transistor;

forming individual conductive metal contacts with said collector plug regions; and

forming an oxide region between said collector plug metal contacts.

CLAIM 9 (original)

The method according to claim 8 wherein said N, N+, P and P+ regions are created through ion implantation.

CLAIM 10 (original)

The method according to claim 8 wherein arsenic ion implantation is used to produce said N-type and N+-type regions.

CLAIM 11 (original)

The method according to claim 8 wherein boron ion implantation is used to produce said P-type and P+-type regions.